METHOD AND APPARATUS UTILIZING MONOCRYSTALLINE INSULATOR

FIELD OF THE INVENTION

The invention relates generally to semiconductor devices, methods, and systems.

BACKGROUND OF THE INVENTION

Semiconductor devices typically comprise multiple layers of conductive, insulative, and semiconductive layers. Crystalline materials, such as silicon, are often employed to serve various functions, especially in the semiconductor and insulator materials. Various properties of such layers tend to improve with the crystallinity of the layer. For example, electron charge displacement and electron energy recoverability of an insulative layer improve as the crystallinity of the layer increases. The amount of charge that can be stored is a function of the dielectric constant of the insulative layer. Further, improved insulative properties tend to reduce the power consumption and size of various components, such as capacitors.

For example, a capacitor generally comprises two conductive elements separated by a dielectric layer. Single-crystal materials exhibit excellent insulative properties, but efforts to construct capacitors with single-crystal dielectric layers have not been particularly successful. These attempts have generally been unsuccessful, at least in part, because lattice mismatches between the host crystal and the grown crystal cause the resulting layer to be of low crystalline quality. Such efforts commonly result in polycrystalline dielectric materials, and the insulating properties of such materials are compromised by defects and grain boundaries. Defects and grain boundaries tend to allow greater leakage current through the dielectric layer, degrading the effectiveness of the insulator. Consequently, conventional devices typically include additional protection layers to prevent the inclusion of foreign materials, defects, and grain boundaries.

To reduce the leakage current, many capacitors include additional dielectric layers, typically formed from amorphous materials, such as amorphous zirconium titanate. Adding layers, however, requires additional processing steps and materials. Further, the properties of such layers are more difficult to control than crystalline materials.

SUMMARY OF THE INVENTION

A semiconductor method and apparatus according to various aspects of the present invention may include a capacitor having a substantially monocrystalline material exhibiting a relatively high dielectric constant. The semiconductor apparatus and method may further include a supplemental layer having a depletion zone, suitably comprised of a high-resistivity material. To facilitate the growth of the insulator and/or other layers, the various layers are suitably lattice matched. Further, the apparatus may include one or more interface layers to facilitate lattice matching of the various layers.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 illustrates a cross-section of a semiconductor apparatus according to various aspects of the present invention having a substantially monocrystalline dielectric layer;

FIGs. 2, 3, 4, and 5 illustrate schematically, in cross section, device structures in various stages of layer preparation;

FIG. 6 illustrates a cross-section of a semiconductor apparatus having an interface layer;

FIG. 7 illustrates a cross-section of a semiconductor apparatus having a supplemental layer for forming a depletion zone;

FIG. 8 illustrates a cross-section of a semiconductor apparatus having a supplemental layer for forming a depletion zone and an interface layer;

FIG. 9 illustrates, in two dimensions, the lattice structures of the (100) surfaces of a substrate, a high-resistivity layer, and a dielectric layer;

FIG. 10 illustrates lattice structures for a substrate, a high-resistivity layer, an interface layer, and a dielectric layer;

FIG. 11 illustrates a cross-section of a semiconductor apparatus having multiple devices;

FIG. 12 illustrates a cross-section of a semiconductor apparatus having multiple capacitors;

FIG. 13 is a flow diagram illustrating a method for fabricating a semiconductor apparatus according to various aspects of the present invention;

FIG. 14 is a flow diagram of an alternative method for fabricating a semiconductor apparatus; and

FIGs. 15 and 16 are performance plots for a voltage variable capacitor constructed in accordance with various aspects of the present invention.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

The subject matter of the present invention is particularly suited for use in connection with semiconductor devices, such as semiconductor capacitors. As a result, the preferred exemplary embodiment of the present invention is described in that context. It should be recognized, however, that such description is not intended as a limitation on the use or applicability of the present invention, but is instead provided merely to enable a full and complete description of a preferred embodiment. Various aspects of the present invention may be applied to a variety of semiconductor devices, such as insulators for devices like insulated gate transistors or other components using high dielectric materials.

A system according to various aspects of the present invention may include one or more semiconductor devices. In the present embodiment, the semiconductor devices include capacitors. Generally, capacitors comprise two conductive elements, such as substantially conductive or semiconductive materials, separated by an electrical

insulator. A system according to various aspects of the present invention may include a semiconductor device having a voltage variable capacitor, also known as a varactor, variable capacitance diode, or varacap, which suitably comprises a semiconductor device characterized by voltage sensitive capacitance that resides in the space-charge region at the surface of a semiconductor bounded by an insulating layer. To form a high performance voltage variable capacitor, a dielectric film, suitably having a sufficiently thin cross section and adequate integrity, may be provided on the semiconductor.

Referring to FIG. 1, a semiconductor device according to various aspects of the present invention includes a capacitor 23. The capacitor 23 suitably comprises a first conductive element, such as a semiconductor substrate 45, and a dielectric layer 42 having a relatively high dielectric constant formed on top of the semiconductor substrate 45 as the insulator. A second conductive element, such as a top electrode 41, is formed on the dielectric layer 42.

The first conductive element may be comprised of any appropriate materials, for example silicon or gallium arsenide. The substrate 45, for example, may be conventionally doped, such as with n+ doping, or comprise multiple materials to achieve desired electrical properties. Further, the substrate 45 may be uniformly doped, or may have areas of greater concentration of dopants to achieve any appropriate electrical characteristics. Similarly, the second conductive element comprises any suitable material, such as a highly conductive material for a capacitor. In the present embodiment, the electrode 41 comprises a conductive metal such as platinum, copper, gold, silver, or aluminum, or may comprise other conductive or semiconductive materials, such as polysilicon or a conductive oxide. The electrode 41 is electrically coupled to an electrode connection 31 and the substrate 45 is electrically coupled to a substrate connection 35.

The dielectric layer 42 separates the substrate 45 and electrode 41. The dielectric layer 42 comprises any suitable material for inhibiting current between the substrate 45 and the electrode 41, such as an alkaline earth metal oxide. In the present embodiment, the dielectric layer 42 comprises a substantially monocrystalline film of any suitable material. Dielectric layer 42 may be, in various embodiments, a

monocrystalline oxide or nitride material selected for its crystalline compatibility with the underlying substrate and with the overlying material layer, as well as its insulating properties. For example, the material may be an oxide or nitride having a lattice structure closely matched to the substrate.

In accordance with various aspects of the present invention, dielectric layer 42 comprises a substantially monocrystalline film of strontium titanate. Monocrystalline films of dielectric materials typically exhibit higher dielectric constants than amorphous or polycrystalline films of the same material. In alternative embodiments, the dielectric layer 42 is formed from any appropriate substantially monocrystalline material having various desired properties, such as resistivity, heat resistance, lattice coefficients, and the like. For example, the dielectric layer 42 may comprise a metal oxide compound, such as barium, strontium, titanium, zirconium, lanthanum, or aluminum, or a combination of one or more of these metals and/or other materials. Strontium titanate ($SrTiO_3$), for example, has a dielectric constant of over 200 in monocrystalline form. Other suitable materials for dielectric layer 42 include $BaTiO_3$, $LaAlO_3$, $SrZrO_3$, $BaZrO_3$ and MgO. Materials that may be suitable for the dielectric layer include, but are not limited to, metal oxides such as alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide, and/or alkaline earth oxides. Additionally, various nitrides such as gallium nitride, aluminum nitride, and boron nitride may also be used for the dielectric layer 42. Generally, these materials are metal oxides or metal nitrides, and more particularly, these metal oxide or nitrides typically include one or two different metallic elements. In some applications, the metal oxides or nitrides may include three or more different metallic elements.

The dielectric layer 42 may be formed according to any suitable technique, such as molecular beam epitaxy, vapor phase epitaxy, pulsed laser deposition, sputtering, evaporation, chemical vapor deposition, ion beam, plasma, sol-gel, or solution chemistry processes. Various suitable processes for forming the dielectric layer 42, for

example, are described in U.S. Patent No. 6,022,410, issued February 8, 2000, to Yu, et al.; U.S. Patent No. 6,113,690, issued September 5, 2000, to Yu, et al.; U.S. Patent No. 6,224,669, issued May 1, 2001, to Yu, et al.; and U.S. Patent No. 6,241,821, issued June 5, 2001, to Yu, et al. For example, referring to FIG. 2, a native oxide 11 may exist on the surface of the substrate 45 from exposure to ambient air. The native oxide typically has a thickness in the range of 10 to 30 Å. The native oxide layer 11 is suitably removed to provide an ordered crystalline surface on the substrate 45 for nucleation of the dielectric layer 42. Thicker native oxide layers tend to require longer exposure to the selected conversion material. To remove the native oxide and expose the monocrystalline surface on the substrate 45, the silicon substrate 45 and amorphous native oxide layer 11 are heated to a temperature below the sublimation temperature of the native oxide layer 11. Generally, the native oxide sublimes at a temperature in excess of 850 °C, so that silicon substrate 45 is heated, preferably, to a temperature in a range of about 700 °C to 800 °C at reduced pressure, such as in the range of approximately 10^{-9} to 10^{-10} Torr.

The surface of the silicon substrate 45 having the native oxide layer 11 is suitably exposed to a beam of a conversion material 14 (FIG. 3) for removing the native oxide layer and forming a template layer for the dielectric layer 42, such as an alkaline earth metal or a combination of an alkaline earth metal and oxygen. For example, the conversion material 14 may comprise barium, strontium, or a combination of the two that is generated by resistively heating effusion cells or from e-beam evaporation sources.

In the present exemplary embodiment, silicon substrate 45 and native oxide layer 11 are exposed to a beam of strontium. The strontium aids in desorption of the native oxide layer 11 at lower temperatures than would otherwise be required. An amount of strontium remains on the silicon surface to form a template layer 12 such as may be indicated by a (2x1) reconstruction in a Reflection High Energy Electron Diffraction (RHEED) pattern. As the amorphous native oxide layer 11 is exposed to a beam of alkaline earth metal(s), the surface is preferably monitored using RHEED techniques which can be used in situ, i.e. while performing the exposing step, for

example within a growth chamber. The RHEED techniques are used to detect or sense surface crystalline structures and, in the present embodiment, change rapidly from diffuse background for the amorphous silicon oxide to strong and sharp streaks upon the completion of the native oxide desorption process. Once a specific manufacturing process is provided and followed, however, it may not be necessary or desirable to perform the RHEED techniques on every substrate.

The cleaned silicon substrate is then lowered to between 200 °C and 600 °C. A $SrTiO_3$ layer 42 may then be deposited on the template layer 12 by exposing it to a beam of strontium, titanium and oxygen. Referring to FIG. 4, a high dielectric crystalline material 42 is deposited on the template layer 12. By controlling the partial pressure of oxygen during the growth of the crystalline material 42, an optional amorphous interface layer 16 can be formed between the silicon substrate 10 and the dielectric 42 as shown in FIG. 5. The amorphous interface layer 16 is formed by oxygen diffusing through the dielectric 42 and reacting with the surface of the silicon substrate 45. Even though the amorphous interface layer 16 is formed at the interface between the silicon substrate 45 and the dielectric layer 42, the dielectric layer still remains single crystalline. The formation of the amorphous interface layer 16 can consume a portion of the silicon surface, or the template layer 12, or a portion of the crystalline material 42.

To facilitate or enhance the growth of other layers, a semiconductor system in accordance with various aspects of the present invention may also include one or more interface layers. Interface layers may be formed between some or all of the various layers, and suitably comprise additional layers of crystalline materials. For example, referring to FIG. 6, an alternative embodiment of a capacitor 24 includes an interface layer 43 formed between the semiconductor substrate 45 and the dielectric layer 42. The interface layer 43 may be formed in any suitable manner, for example in the same manner as the dielectric layer 42. In the present embodiment, the interface layer 43 suitably comprises a monocrystalline material, suitably a different material than used to form the substrate 45 and the dielectric layer 42. The interface layer 43 assists in the

proper formation of the subsequent dielectric layer, suitably acting as a template layer for subsequent growth of the dielectric layer 42.

In semiconductor devices according to various aspects of the present invention, the crystalline structures of a first layer such as a high-resistivity layer 44 (described below) or semiconductor substrate 45, a second layer such as the dielectric layer 42, and in some embodiments a third layer, such as the interface layer 43, may be substantially matched. For example, the interface layer 43 may be substantially lattice matched to the substrate 45 and the dielectric layer 42. The interface layer 43 suitably has a lattice constant slightly higher than that of the substrate 45 and slightly lower than that of the dielectric layer 42, or is suitably oriented at an angle to the lattice of the substrate to assist in obtaining a desired orientation of the dielectric layer 42.

Referring to FIGs. 9 and 10, in an embodiment having the dielectric layer 42 directly atop the semiconductor substrate 45 or a high-resistivity layer 44 (e.g. as shown in FIGs. 1 and 7, respectively), the semiconductor substrate 45 and the high-resistivity layer 44 are comprised of silicon having a lattice constant of 5.43 angstroms, and dielectric layer 42 is comprised of strontium titanate ($SrTiO_3$) having a lattice constant of 3.9 angstroms. For the strontium titanate film of dielectric layer 42 to match the silicon lattice of substrate 45 or high-resistivity layer 44, the crystalline structure of dielectric layer 42 may be rotated at an angle, such as 45 degrees, relative to the silicon lattice of the high-resistivity layer 44 or semiconductor substrate 45 normal to the (100) growth direction. For example, suitable materials and techniques for orienting a layer with respect to another are described in U.S. Patent No. 6,241,821, issued to June 5, 2001 to Yu, et al., and U.S. Patent No. 6,248,459, issued June 19, 2001, to Wang, et al. At an angle of 45 degrees, the relative lattice constant of strontium titanate (3.90 angstroms x 1.414 = 5.51 angstroms), is comparable to the lattice constant of silicon (5.43 angstroms). In one embodiment, the lattice constants of the respective layers are within about 2%.

In an alternative embodiment including an interface layer 43 (e.g. as shown in FIGs. 6 and 8), the interface layer 43, suitably comprising strontium silicate (in which silicon, strontium, and oxygen atoms are bonded to form a (2x1) structure), strontium

oxide, or other appropriate material, promotes the growth of the strontium titanate dielectric layer 42 in a 45-degree rotation with respect to the silicon high-resistivity layer 44 or substrate semiconductor substrate 45. Interface layer 43 may be as thin as a single layer of atoms.

A capacitor according to various aspects of the present invention may also be configured to include a supplemental layer for forming a depletion zone while the capacitor is operating. For example, referring to FIG. 7, a voltage-variable capacitor (VVC) 21 may include a supplemental layer, suitably comprising an epitaxial layer of high-resistivity semiconductor material 44, such as lightly doped single-crystal silicon, formed into the substrate 45 or positioned atop the substrate 45. Alternatively, the supplemental layer may be formed in conjunction with an interface layer 43 (FIG. 8) to facilitate the growth of the dielectric layer 42 over the supplemental layer.

The supplemental layer may serve as an area for a depletion zone 47 (often referred to as a barrier layer, a blocking layer, or a space-charged layer) to form, which facilitates a voltage-variable characteristic for the VVC 21. The depletion zone 47 is a transient layer formed when a bias voltage is applied to the capacitor. The depletion zone 47 may change or disappear when the applied voltage field is varied or removed. Depletion zone 47 is a region of net space-charge in a semiconductor in which the density of mobile charge elements tends to be significantly less than the density of ionized impurity atoms. The mobile carrier charge density is insufficient to neutralize the fixed charge density of donors and acceptors.

High-resistivity layer 44 may be formed or deposited in any suitable manner, such as by epitaxially growing the layer 44 on the semiconductor substrate 45, counter-doping the substrate 45, conventional photolithography and etching, or ion implantation. In the present embodiment, the high-resistivity layer 44 is preferably less heavily doped (n-) than heavily doped (n+) semiconductor substrate 45, and has a higher resistivity than semiconductor substrate 45. The thickness of the high-resistivity layer 44 may be chosen to be equal to or slightly greater than a maximum depletion width to minimize the series resistance of VVC 22 while maximizing the capacitance change. A lower doping level of high-resistivity layer 44 facilitates faster formation of

the depletion zone 47. The physical thickness of the high-resistivity layer 44 provides a limitation on the maximum thickness of the depletion zone 47, thus providing a controlled maximum value to the variable capacitance.

In operation, a voltage is typically applied across VVC 21 by applying the voltage across connections 31, 35. The capacitance of the VVC 21 is controlled by adjusting the voltage applied across the connections 31, 35. When an appropriate voltage is applied to the connections 31, 35, depletion zone 47 forms which extends for a selected distance into the high-resistivity layer 44. The depletion zone 47 behaves as a variable capacitance electrically in series with the constant capacitance formed by the electrode 41 and the substrate 45. The two capacitances create a net capacitance effect that is affected by the width of the depletion zone 47. The bias voltage applied across connections 31, 35 controls the width of the depletion zone 47.

A semiconductor device according to various aspects of the present invention may be fabricated in any suitable manner to achieve the desired characteristics of the device and form the desired layers. For example, referring to FIG. 13, a semiconductor device may be formed by doping the substrate 45 (step 1202), such as a silicon substrate; depositing the single-crystal dielectric layer 42 on the substrate 45 (step 1208), the dielectric layer 42 having a lattice constant substantially matching that of the semiconductor substrate 45; and forming an electrode 41 on the dielectric layer 42 (step 1210). The step of doping the substrate 45 may comprise n+ doping the substrate 45. The process may further include a step of forming an interface layer 43 between the substrate 45 and the dielectric layer 42 (step 1206).

The fabrication process may further include a step of forming the high resistivity layer 44 on the substrate 45 (step 1204). The high resistivity layer 44 (as well as the other layers of the device) is suitably epitaxially grown silicon and lightly n doped, which may then be selectively removed using conventional photolithography and etching. In another embodiment, the step of forming the high resistivity layer 44 may include ion implantation of doping impurities. An interface layer 43 may also be formed on the high resistivity layer (step 1206), such as by forming a single crystal material which is substantially lattice matched to the substrate 45.

Referring to FIG. 14, an alternative method for fabricating a device, such as a capacitor, comprises the steps of: providing a silicon substrate 45; heavily doping a region of the silicon substrate 45 (step 1302); forming silicon dioxide on a surface of the region (step 1304); heating the silicon substrate to a temperature below the sublimation temperature of the silicon dioxide (step 1306); exposing the surface of the region to a beam of alkaline earth metal (step 1308); depositing a high dielectric constant material 42 (step 1310); and forming an electrode 41 on the region (step 1312). In another embodiment, the surface of the region is exposed to beams of alkaline earth metal and oxygen; depositing a high dielectric constant material 42; and forming an electrode 41 on the region. The silicon substrate 45 is preferably maintained through all the steps at a temperature below 850 °C, and the step of heating the silicon substrate to a temperature below the sublimation temperature of the silicon dioxide is suitably accomplished by heating the silicon substrate to a temperature between 700 °C and 800 °C. In addition, the step of exposing the surface of the doped region to a beam of alkaline earth metal or beams of alkaline earth metal and oxygen may be performed at a reduced pressure, for example in the range of 10^{-7} to 10^{-10} Torr. Surface structures during these steps may be monitored with RHEED techniques.

Various aspects of the present invention may be applied to integrated circuits of multiple devices, including capacitors in integrated circuits. Additionally, monocrystalline dielectric layers may be deposited on substrates commonly used in the semiconductor industry such that capacitors or VVCs may be integrated with other elements of integrated circuits such as transistors. This allows for the integration of an RF front-end module on a single chip. In this embodiment, the substrate is silicon but could also be chosen from the group III-V semiconductors.

For example, referring to FIG. 11, an integrated circuit suitably includes a voltage-variable capacitor (VVC) 25 and another device 27, such as a MOS transistor. The VVC 25 according to the present embodiment includes a heavily doped (n+) region 46 in the semiconductor substrate 45. The VVC 25 suitably includes a high-resistivity layer 44 that covers the doped region 46. Doped region 46 may be electrically attached to connection 36 by means of an n+ doped region 50 so that voltage may be applied

across capacitor 25 via connections 31, 36. The VVC 25 further suitably includes an interface layer 43 to assist in the proper formation of the dielectric layer 42 in the desired orientation.

Other doped regions 48 may also be included in the substrate 45 to provide other devices 27. For example, device 27 may be a field effect transistor, including a gate insulator 51, a gate electrode 52, a gate terminal 54, a source/drain implant region 53, and source and drain electrodes 55, 56. The fabrication of such field effect transistors on a substrate may be performed in any suitable manner, such as according to conventional fabrication techniques. Other devices 27 also suitably comprise other semiconductor components that may be formed within or placed on the other doped regions similar to doped region 48 of semiconductor substrate 45 to form other devices 27. The other semiconductor devices 27 and other semiconductor components may be connected to VVC 25 to form integrated circuits. Such a voltage variable capacitor may be utilized, for example, in an integrated circuit that tunes a frequency dependent portion of a radio circuit. For example, the VVC can be coupled to another capacitor in an oscillator. By varying the voltage on the VVC, the capacitance changes, thus shifting the frequency of the oscillator. The voltage to the capacitor can be changed under control of a transistor that is fabricated upon the same substrate as the VVC.

Referring to FIG. 12, in another embodiment according to various aspects of the present invention, a semiconductor device may include a capacitor array 26 comprising a plurality of capacitors 24. The capacitors 24 in capacitor array 26 may have different size electrodes 41 resulting in different capacitances. Further, the capacitors 24 in capacitor array 26 may be connected or unconnected to each other to provide desired characteristics.

The substrate 45 may include a heavily doped (n+) region 46 shared by multiple components. In addition, the capacitor array 26 may include the interface layer 43 to assist in the proper formation of the subsequent dielectric layer 42 in the proper orientation, which may also be shared by multiple capacitors 24. Other layers, such as a high-resistivity layer (not shown), may be shared among one or more capacitors as well. The shared doped region 46 is suitably electrically coupled to the connection 36. Thus,

the capacitors in capacitor array 26 share a common connection 36, but each has its own electrode connection 31.

EXAMPLE

FIG. 15 shows a capacitance versus voltage plot and FIG. 16 shows a leakage current versus voltage plot for a voltage variable capacitor constructed in accordance with various aspects of the present invention. The capacitor includes a high-resistivity layer 44 such as is described in FIG. 7. The thickness of the strontium titanate insulating layer is 1000 angstroms. The silicon substrate is heavily n+ doped, with a light n doped epitaxial high resistivity layer. The resulting capacitance is 0.65uF/cm2, which is more than twice that of conventional voltage variable capacitors made from amorphous or polycrystalline zirconium titanate. The leakage current is 3E-4mA/cm2 compared to leakage currents of about 0.5mA/cm2 for conventional VVCs. The substantially reduced leakage is a result of the substantially single crystal dielectric which is lattice matched to the substrate, resulting in a substantially continuous crystal structure with substantially no dangling bonds, dislocations, grain boundaries, and the like.

Using high quality monocrystalline material, a variety of semiconductor devices may be fabricated in or use that film at a low cost compared to the cost of fabricating such devices beginning with a bulk wafer of semiconductor material or in an epitaxial film of such material on a bulk wafer of semiconductor material. In addition, a thin film of high quality monocrystalline material may be realized beginning with a bulk wafer such as a silicon wafer, such that an integrated device structure could be achieved that takes advantage of the properties of both the silicon and the high quality monocrystalline material. A capacitor, such as a voltage variable capacitor, may be created using the properties of the monocrystalline material in the insulator of the capacitor. The insulator comprises a substantially monocrystalline material having a relatively high dielectric constant. The semiconductor apparatus may further include a supplemental layer having a depletion zone, suitably comprised of a high-resistivity material, for forming a voltage-variable capacitor. To facilitate the growth of the insulator and/or other layers, the various layers are suitably lattice matched. Further,

the apparatus may include one or more interface layers to facilitate lattice matching of the various layers.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.